

1 **INTEGRATED PC CARD HOST CONTROLLER FOR THE DETECTION AND**
2 **OPERATION OF A PLURALITY OF EXPANSION CARDS**

3 This application is a continuation application under 37 CFR §1.53(b) of copending
4 application Serial No. 09/536,578, filed March 28, 2000 and assigned to the same assignee,
5 which is hereby incorporated by reference in its entirety.

6 **1. Field of the Invention**

7 The present invention relates to an integrated controller for the detecting and operating
8 one or more expansion cards. More specifically, the present invention relates to an integrated
9 controller for detecting and controlling PC Cards (16-bit PCMCIA cards and 32 bit-CardBus
10 cards), and smart cards. Particular utility of the present invention is to provide an integrated
11 controller for mobile computing devices, e.g., laptop computers, etc, although other utilities are
12 contemplated herein.

13 **2. Description of Related Art**

14 The need for security and enhanced privacy is increasing as electronic forms of
15 identification replace face-to-face and paper-based ones. The emergence of the global Internet,
16 and the expansion of the corporate network to include access by customers and suppliers from
17 outside the firewall, have accelerated the demand for solutions based on public-key technology.
18 A few examples of the kinds of services that public key technologies enable are secure channel
19 communications over a public network, digital signatures to ensure image integrity and
20 confidentiality, and authentication of a client to a server (and visa-versa).

21 Smart cards are a key component of the public-key infrastructure that Microsoft is
22 integrating into the Windows platform because smart cards enhance software-only solutions such
23 as client authentication, logon, and secure e-mail. Smart cards are essentially a convergence
24 point for public key certificates and associated keys because they provide tamper-resistant

storage for protecting private keys and other forms of personal information; isolate security-critical computations involving authentication, digital signatures, and key exchange from other parts of the system that do not have a "need to know"; and enable portability of credentials and other private information between computers at work, home, or on the road.

It is estimated that the smart card will become an integral part of the Windows platform because smart cards will enable new breeds of applications in the same manner that the mouse and CD-ROM did when they were first integrated with the Personal Computer (PC). Incompatibility among applications, cards, and readers has been a major reason for the slow adoption of smart cards outside of Europe. Interoperability among different vendors' products is a necessary requirement to enable broad consumer acceptance of smart cards, and for corporations to deploy smart cards for use within the enterprise.

ISO 7816, EMV, and GSM

In order to promote interoperability among smart cards and readers, the International Standards Organization (ISO) developed the ISO 7816 standards for integrated circuit cards with contacts. These specifications focused on interoperability at the physical, electrical, and data-link protocol levels. In 1996, Europay, MasterCard, and VISA (EMV) defined an industry-specific smart card specification that adopted the ISO 7816 standards and defined some additional data types and encoding rules for use by the financial services industry. The European telecommunications industry also embraced the ISO 7816 standards for their Global System for Mobile communications (GSM) smart card specification to enable identification and authentication of mobile phone users.

While all of these specifications (ISO 7816, EMV, and GSM) were a step in the right direction, each was either too low-level or application-specific to gain broad industry support.

1 Application interoperability issues such as device-independent APIs, developer tools, and
2 resource sharing were not addressed by any of these specifications.

3

4 PC/SC Workgroup

5

6 The PC/SC (Personal Computer/Smart Card) Workgroup was formed in May 1996 in
7 partnership with major PC and smart card companies: Groupe Bull, Hewlett-Packard, Microsoft,
8 Schlumberger, and Siemens Nixdorf. The main focus of the workgroup has been to develop
9 specifications that solve the previously mentioned interoperability problems. The PC/SC
10 specifications are based on the ISO 7816 standards and are compatible with both the EMV and
11 GSM industry-specific specifications. By virtue of the companies involved in the PC/SC
12 Workgroup, there is broad industry support for the specifications and a strong desire to move
13 them onto an independent-standards tract in the future.

14 Since its founding and initial publication of the specifications, additional members have
15 joined the PC/SC Workgroup. New members include Gemplus, TBM, Sun Microsystems,
16 Toshiba, and Verifone.

17 Microsoft's Approach

18 Microsoft's approach consists of the following:

- 19 • A standard model for interfacing smart card readers and cards with PCs
- 20 • Device-independent APIs for enabling smart card-aware applications
- 21 • Familiar tools for software development
- 22 • Integration with Windows and Windows NT platforms

23 Having a standard model for how readers and cards interface with the PC enforces
24 interoperability among cards and readers from different manufacturers. Device-independent APIs

1 serves to insulate application developers from differences between current and future
2 implementations. Device-independence also preserves software development costs by avoiding
3 application obsolescence due to underlying hardware changes.

4 The most popular method currently being used to interface a smart card with a notebook
5 computer is to use a PCMCIA Type II smart card reader/writer (Figure 1). PCMCIA smart card
6 readers are currently available from companies such as Gemplus, SCM Microsystems and
7 Tritheim Technologies, to name a few. The end user cost for these smart card readers is typically
8 around \$150. The cost of the reader is a major portion to the cost of the overall security solution.
9 The adapter card 104 in Figure 1 depicts the major functional blocks of a conventional smart card
10 reader. The PCIC Host Interface block of the smart card reader provides the electrical interface to
11 the PC Card connector (106, which in turn connects to the PC Card controller 102. Additional
12 logic is provided to control the interaction between the smart card and the software application.
13 However, as noted above, this solution carries a significant per unit cost, and thus, is an
14 unattractive alternative to large-scale migration to smart card compatibility.

15 Thus, there exists a need to provide an integrated host controller that provides PC Card,
16 smart card, and Passive smart card adapter operability. Moreover, there exists a need to provide
17 an integrated controller that can replace existing motherboard-mounted PC Card host controllers,
18 without having to retool or redesign the motherboard.

19 **SUMMARY OF THE INVENTION**

20 Accordingly, one object of the present invention is to provide an integrated PC Card and
21 Smart card controller suitable to replace conventional PC Card controllers for integration into
22 current PC motherboard technology.

23 It is another object to provide a controller as above that is simultaneously fully

1 compatible with PC Card specifications.

2 It is still another object to provide a Smart card controller, as above, that has an identical
3 pinout arrangement as existing PC Card controllers, thereby permitting the controller to be
4 directly integrated onto a PC motherboard without redesigning and/or retooling costs.

5 It is another object of the present invention to provide logic and methodology to detect
6 the presence of a smart card or a Passive smart card adapter utilizing existing PC Card specified
7 signals.

8 In one aspect, the present invention provides a method of detecting the presence of an
9 expansion card using conventional PC Card specification signal lines, during the initial card
10 detection sequence. The method comprising the steps of determining the signal state of a first
11 and second card detection signal lines; determining the signal state of a first and second voltage
12 select signal lines; determining if said first and/or second card detection signal lines, or said first
13 and/or second voltage select signal lines, comprise a signal state that is reserved by a PC Card
14 signal specification; and determining the signal state of a predetermined unused PC Card signal
15 line, relative to said reserved signal state. During the card detection sequence the status change
16 signal (STSCHG) is used to detect a smart card or a smart card adapter. After the detection
17 sequence is completed the STSCHG signal has the original uses based on the PC Card
18 specification for signal definition. Also, in the preferred embodiment, this process determines
19 the presence of a smart card or a Passive smart card adapter by determining whether said first
20 card detection signal and said second voltage select signals are tied together.

21 In logic form, the present invention provides a device to detect the presence of an
22 expansion card using conventional PC Card specification signal lines, comprising a state
23 machine including a lookup table and a plurality of logic sets, each said logic sets operable to

1 interface with a certain predefined expansion card type, said state machine accepting as input
2 signals a plurality of predetermined card detection and voltage selection signals, and an
3 additional signal, and coupling an appropriate one of said logic sets to an appropriate one of said
4 expansion cards based on a match between said input signals and said lookup table.

5 In another aspect, the present invention provides an integrated circuit for the detection
6 and operation of a plurality of expansion cards, comprising, a first logic set for detecting and
7 operating a plurality of expansion card types, said first logic set having predetermined signal
8 lines and a pinout arrangement defined by PC Card specifications, and a second logic set for
9 detecting and operating a smart card, wherein said first and second logic being incorporated into
10 a single controller without requiring additional pinouts. In the preferred embodiment, the second
11 logic set is adapted to reassign certain ones of said predetermined signal lines to detect and
12 operate said smart card , so that additional pins are not required.

13 It will be appreciated by those skilled in the art that although the following Detailed
14 Description will proceed with reference being made to preferred embodiments and methods of
15 use, the present invention is not intended to be limited to these preferred embodiments and
16 methods of use. Rather, the present invention is of broad scope and is intended to be limited as
17 only set forth in the accompanying claims.

18 Other features and advantages of the present invention will become apparent as the
19 following Detailed Description proceeds, and upon reference to the Drawings, wherein like
20 numerals depict like parts, and wherein:

21 **Brief Description of the Drawings**

22 Figure 1 depicts a block diagram of a conventional solution to incorporate smart card
23 operability for PC applications;

Figure 2 is a system-level block diagram of the integrated smart card reader of the present invention;

Figure 3 is a detailed block diagram of the integrated Smart card reader of the present invention;

Figure 4 is a state machine block diagram of the integrated Smart card reader of the present invention;

Figure 5 is a table of conventional PC Card detection and voltage sensing pin arrangements, and an example of the use of a pin arrangement for smart card detection employed by the controller of the present invention;

Figure 6 is a flowchart of an exemplary smart card and passive smart card adapter detection scheme of the present invention; and

Figures 7A and 7B depict tables showing conventional PCMCIA assigned functional pins and their use for Smart Card interface and detection, respectively.

Detailed Description of Exemplary Embodiments

Figure 2 depicts a system-level block diagram of how the passive smart card adapter and a smart card interface with a host controller. The controller 10 is integrated into a PC platform, for example, laptop PC. As an example, the PC may be configured as shown, with the controller 10 operating to detect and control one or more expansion device cards that are inserted into Socket A 12 and/or Socket B 14. It will be understood that the controller 10 of present invention is adapted with the appropriate logic to drive PC Cards as well as smart cards. The PC system typically includes a processor 26 and a data bus 20. "North Bridge" logic 24 provides communication between the processor 26 and the bus 20. The controller 10, of the present invention is likewise adapted to communicate with the bus 20. In this example, the bus 20 is a

1 PCI bus, however, any bus technology can be incorporated into the controller's logic. To
2 complete the picture, "South Bridge" logic is provided for external bus communications, for
3 example, legacy devices (ISA bus architecture), etc. South Bridge and North Bridge logic are
4 well known in the art. Power IC chip 28 supplies the correct voltages (as determined by the card
5 type inserted into Socket A or B) to the pins of the PC Card connector. Once the type of card is
6 detected (based on the PC Card definitional table of Figure 5, discussed below), chip 28 supplies
7 the appropriate voltage for that card type.

8 In one embodiment, the present invention provides a passive smartcard adapter 18 which
9 is configured to be inserted into either Socket A 12 or Socket B 14, which are in turn configured
10 as either PC Card type I/II/III--type socket interface. The passive adapter 18 of this embodiment
11 includes appropriate connector 84 and passive circuit 86. The smart card 16 inserted into the
12 passive smart card adapter 18 also includes physical contacts 88 to interface with the physical
13 connector 84 of the adapter. Pinout arrangements 84 and 88 of the adapter and smart card are
14 dictated by the smart card specification, for example PC/SC compliant Smart card specification
15 that meets ISO 7816 electrical specifications and T = 0, T = 1 protocols. In this embodiment the
16 use of an adapter 18 permits smart card readability and operability without retooling the PC case
17 to include a specific smart card socket. Alternatively, the PC can include a smart card slot 14' as
18 shown in Figure 2. In this alternative embodiment, the logic 86 and connector 84 are, of course,
19 provided internally within socket 14.

20 Referring now to Figure 3, a more detailed block diagram of the integrated controller 10
21 is depicted, showing those logic portions directed to smart card detection and operability. In this
22 example, the controller 10 includes smart card sensing logic 30A and 30B, Smart card
23 multiplexer (MUX) logic 32A and 32B, Smart card reader logic 34A and 34B and interface logic

1 36Aand36B.

2 It should be noted at the outset that Figure 3 depicts only the logic associated with
3 smartcard and Passive smart card adapter detection and operability, and it should be understood
4 that controller 10 includes additional logic (not shown) to permit detection and operation of
5 conventional PC Card's. Conventional PC Card controllers detect the type of card inserted into a
6 slot using a set of card detection pins, CD 1 and CD2, and a set of voltage sense pins VS 1 and
7 VS2. The coupling combinations between these pins (with reference to ground) indicate to the
8 appropriate logic which type of card has been inserted into the socket. For example, as shown in
9 the table of Figure 5, the coupling combination of CD1, CD2, VS1 and VS2 determine whether
10 the PC Card inserted is a 16-bit PCMCIA card or a 32-bit CardBus card. Moreover, as shown
11 in the table, this combination also determines the driving voltage for the particular type of card.
12 For example, 3.3 V, 5 V, X.X V and Y.Y V. In the last two rows of the table of Figure 5, it is to
13 be noted that the listed combinations of CD1, CD2, VS1 and VS2 are reserved in the PC Card
14 specification. The present invention utilizes one of these reserved combinations of CD 1, CD2,
15 VS1 and VS2, and additionally uses a status change signal, STSCHG, to indicate whether a smart
16 card has been inserted into the slot (either directly, or via an adapter). The status change signal is
17 preferably used in the present invention since this signal is not utilized during the detection
18 process for conventional PC Card cards, and is only used once the card type is known.

19 Thus, in one sense, the smart card sensing logic 30A shown in Figure 3 can be viewed as
20 a state machine that determines the type of card inserted into a socket. To that end, and referring
21 to Figure 4, a state machine representation of the card sensing logic 30A of Figure 3 is depicted.
22 As is shown, the card sensing logic 30A accepts as inputs CD1, CD2, VS1, VS2 and status change
23 (labeled 40, 42, 44, 46 and 48, respectively). In accordance with the reserved arrangement of

1 CD1, CD2, VS1, V52 as shown in Figure 5, and the addition of the status change signal, the state
2 machine 30A determines the appropriate logic 32 A for communicating with the4 given type of
3 card. For example, certain combinations of CD 1, CD2, VS 1, V52 (as indicated in Figure 5) will
4 dictate that the card inserted into the socket is either a 16-bit PC card or a 32-bit CardBus PC
5 card. Accordingly, the state machine 30A will activate the appropriate logic 50 or 52 for the
6 given card type. It should also be noted that the particular voltage of the inserted card is also
7 determined using the combination of these four pins. Extending the capabilities of conventional
8 PC Card controllers, the present invention also monitors the 575 CHG pin to determine if a smart
9 card or a passive smart card adapter has been inserted into the socket, and likewise activates the
10 appropriate logic 54 to communicate with the smart card, for example, logic 32A as shown in
11 Figure 3. To determine the states of CD1, CD2, VS1, V52 and STSCHG, the card sensing logic
12 30A can produce, for example, a pulse train signal on selected ones of these pinouts, and by
13 monitoring the signal on one or more of the other pins (with respect to ground), it can then be
14 determined the card type inserted into the socket.

15 The smart card sensing logic 30A and 30B operate to detect both a smart card or a
16 passive smart card adapter and PC Cards, based on the Table in Figure 5. The pin assignments
17 shown in Figure 5 are designated by the PC Card specification, and are conventional pin
18 assignments for these signal lines. The identity of the card is determined by the values of the
19 voltages of columns 1-4, i.e., CD2, CD1, V52 and VS1. Both smart card and passive smart card
20 adapter detection operates by utilizing the reserved combinations of these pins, plus the use of an
21 additional pin, for example, STSCHG signal line. The concept is summarized in the Table of
22 Figure 7B. This table shows the pins used to detect PC Cards, smart cards and Passive smart card
23 adapter cards. The signal column for a smart card or passive smart card adapter detection

1 includes one of the reserved areas for CD1, CD2, VS1 and V52, as shown in the last two rows of
2 Table of Figure 5. It should be noted that although the figures depict the use of signal line
3 STSCHG (which is provided by the conventional PC Card specification), the present invention,
4 generally, could use any pin in the PC Card specification that is unused during the card detection
5 sequence. In other words, from a timing perspective, certain signal lines in the PC Card
6 specification remain unused during the card detection process. The present invention utilizes one
7 (or more) of these signal lines, in conjunction with the reserved combination of CD1, CD2, VS1,
8 and V52, to effectuate smart card or passive smart card adapter detection. Thus, the figures
9 represent only one of many examples for the use of an additional signal pin that could be used
10 for smart card detection.

11 A flow chart 60 of the card-type detection process is depicted in Figure 6. For clarity, the
12 corresponding reference numerals of the logic to detect and operate PC Card, smart card and
13 passive smart card adapter cards (as shown in Figures 2 and 3) are omitted. Initially, the
14 detection logic seeks the presence of CD1, CD2, VS1, V52, and STSCHG 62. If not present, or
15 otherwise unavailable, it is assumed the no card has been inserted into a socket, and thus the card
16 detection signals (CD1 and CD2) are blocked 64. Once a card is inserted, the detection logic
17 monitors the falling edge of CD1 or CD2 66. This is dictated by the PC Card specification for
18 determining the presence of a card. Once a card is detected, the detection logic of the present
19 invention toggles CD1, CD2, VS1, V52, and STSCHG to determine the type of card inserted 68.
20 Toggling, as cited above, can be in the form of a pulse train signal, or other toggling signal. The
21 detection logic proceeds by polling CD 1, CD2, VS 1, V52, and STSCHG in the following
22 manner. First, the logic determines if VS1 and CD2 are tied to ground 70. If not, it is known that
23 a 16-Bit PCMCIA Card or 32-bit CardBus card is inserted 72, as indicated by the table of Figure

1 5. If yes, the logic determines if V52 and CD1 are tied together 74. If this is not the case, again it
2 is known that a 16-Bit Card or 32-bit CardBus card is inserted 76, as indicated by the table of
3 Figure 5. If it is determined that CD1 and STSCHG are tied together 78, then it is determined that
4 a smart card or a passive smart card adapter is present. Either the passive smart card adapter is
5 inserted into the socket, or a smart card is inserted directly into a smart card socket 82.

6 Another feature of the present invention is to provide an integrated controller circuit 10,
7 which can be directly integrated with current PC Card controller logic. Conventional PC Card
8 controller logic is an IC package that is mounted directly on the motherboard, which has 208
9 pins, and each of these pins is assigned by the PC Card specification. Another feature is to
10 provide a controller 10 that can directly replace conventional controllers, without having to
11 reconfigure pin assignments, add additional pin configurations, alter the motherboard, or change
12 the tooling required. To that end, and referring to the table of Figure 7A, the controller 10 of
13 present invention includes both conventional, legacy interface card signals and smart card
14 signals. As is shown in this table, the same pins (leftmost column) used to interface with
15 conventional 16 and 32 cards are likewise used to interface with the smart card. Thus, no
16 additional pins are required. Referring again to Figure 3, if a smart card is detected into a socket,
17 logic 30A or 30B communicates with and enables logic 34A or 34B, to enable smart card
18 readability. Logic 34A and 34B enable the socket MUX logic 32A or 32B, so that the socket (A
19 or B) can communicate with the cardbus/PCI controller logic 36A or 36B, which communicate
20 with the PCI bus 20 (via PCI interface 38). As should be understood, the smart card logic 30A,
21 30B, 34A and 34B of the present invention directly interfaces with the MUX logic 32A and 32B
22 and communicates with bus interface controllers 36A and 36B using conventional PC Card 2
23 communication protocols. If a conventional card is inserted into a socket (socket A or B), then

1 conventional logic (not shown) incorporated into the controller 10 activates MUX 32A and 32B
2 and communicates with bus interface controllers 36A and 36B using conventional PC Card
3 communication protocols.

4 To facilitate direct integration with conventional PC Card logic sets, the present invention
5 controls a predetermined number of pre-assigned pins to effectuate smart card communication.
6 For example, as shown in Figure 7A, pins 17, 51, 58, 47, 32, GND, 18, 16 and 40, as specified
7 by the PC Card standard, are utilized by the present invention to operate both smart cards and PC
8 cards. Therefore, no extra pins are required by the controller 10 to effectuate Smart card
9 operability. In operation, once the smart card has been detected (as described above with
10 reference to Figures 3-6), logic 34A or 34B reassigns the operability of the PC Card pins noted in
11 Figure 7A to effectuate Smart card readability. The signal assignments, set forth under the smart
12 card Signal column of Figure 7A, are the required signals to read smart Cards.

13 The table and Figure 7A is included as a lookup table in the controller 10 of the present
14 invention to operate PC Cards. Likewise, the tables of Figure 5 and Figure 7B are included as
15 lookup tables in the controller 10 for the detection of PC Cards and smart Cards. To this end, and
16 view the logic sets 30A and 30B as a state machine (shown in Figure 4), the state machine
17 compares the input signals to the lookup tables of Figures 5 and 7B to couple the appropriate
18 logic to the card.

19 Those skilled in the art will recognize that CDI, CD2, VS1 and V52 comprise card detect
20 and voltage select signals, respectively, as specified by the conventional PC Card signal
21 specification. In the tables of Figures 5, 7A and 7B, and the flowchart of Figure 6, the
22 nomenclature used for these signal lines includes, for example, CDI#, CD2#, VS 1#, V52#, etc.,
23 which are the formal names for these conventional signal lines. However, it should be apparent

1 that the use of CD1, CD2, VS1 and V52 are shorthand versions of these formal names, and may
2 be used interchangeably.

3 Thus, it is evident that there has been provided an integrated Smart card controller and
4 Smart card detection process that satisfies the aims and objectives stated herein. It will be
5 apparent to those skilled in the art that modifications are possible. For example, although the
6 present invention has been described with reference to detection and operation of smart Cards,
7 the present invention is equally adapted for the detection and operation of any type of expansion
8 cards, in addition to conventional PC Cards. Other modifications are possible. For example, it
9 may be desirable to include a software lock on the operability of the smart card logic shown
10 herein. Accordingly, the logic depicted in Figure 3 can include an enable bit, which selectively
11 turns on and off smart card detectability and operability. To that end, and referring to Figure 6,
12 the smart card detection process may alternatively include the step of determining if an enable bit
13 is enabled, and if CD1 and STSCHG are tied together 84. If this is not the case, the smart card
14 the logic will not detect the presence of a smart card. This feature of the present invention
15 permits, for example, manufacturers to offer smart card compatibility as an upgrade option,
16 while still integrating the core logic of the controller 10. Those skilled in the art will recognize
17 additional modifications, and all such modifications are deemed within the scope of the present
18 invention, only as limited by the appended claims.